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MODIFIED TOPOLOGY FOR DSTATCOM WITH REDUCED FILTER SIZE AND VSI RATING

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Abstract: *Design of voltage source inverter and the interfacing filter are two important issues while implementing DSTATCOM. In this paper, a new DSTATCOM topology has been proposed which reduces the rating of VSI as well as the size of interfacing filter. In order to reduce the rating of VSI, a capacitor is used in series with the interfacing filter, which reduces the dc link voltage, which in turn reduces the rating of VSI, as rating of VSI is proportional to dc link voltage. A traditional L filter is replaced with LCL filter, which reduces the size of interfacing filter. An LCL filter provides excellent switching harmonics elimination capability as compared to conventional L filter. Therefore, proposed topology will reduce weight, cost, rating, and size of the DSTATCOM as compared to conventional topology. Effectiveness of the proposed DSTATCOM topology over traditional topology is verified through MATLAB/Simulink.*

Keywords: *DSTATCOM, dc link voltage, L filter, LCL filter, series capacitor.*

I. INTRODUCTION

THE proliferation of power electronics devices, nonlinear loads, and unbalanced loads has degrades the power quality in the power distribution network. Switching devices such as uninterrupted power supplies, arc furnaces draw reactive and harmonics power from supply mains. They cause power quality problems such as poor power factor, high harmonics and unbalanced source currents. When the unbalanced source currents flow through the feeder impedance, make the load voltage or point of common coupling (PCC) unbalanced as well as distorted.

A distribution static compensator (DSTATCOM) is a shunt active power filter connected at the PCC in a distribution system, which injects currents into the PCC, such that the harmonic filtering, power factor correction, and load balancing can be achieved.

. Generally while implementing in real time, DSTATCOM suffers from high power rating requirement. Load current to be compensated and dc link voltage is directly proportional to the power rating of the shunt active power filter. The compensation performance of any active filter depends on the voltage rating of dc-link capacitor. In general, the dc-link voltage has much higher value than the peak value of the line-to-neutral voltages. The primary condition for reactive power compensation is that the magnitude of reference dc-bus capacitor voltage should be higher than the peak of source voltage at the PCC. In order to achieve satisfactory compensation, the dc link voltage has much higher value than the maximum of phase voltage. Rating of VSI increases due to increase in dc link voltage, makes VSI more bulky, IGBT switches must be rated for higher value of voltage and current. Therefore, the cost, weight, and power rating of VSI increases.

In conventional DSTATCOM topology, For shaping of the injected currents, an L filter is used at front of VSI. However, L filter uses a bulky inductor, which produces large voltage drop across it, so for proper compensation it requires higher value of dc link voltage. In order to reduce the size and power rating of SAPF, several topologies have been proposed where a passive components is used with active filter[10]-[12]. To have a reduced dc-link voltage without compromising the compensation capability, uses a series capacitor along with the interfacing inductor and a shunt filter capacitor. With the reduction in dc-link voltage, the average switching frequency of the insulated gate bipolar transistor switches of the DSTATCOM is also reduced. Consequently, the switching losses in the inverter are reduced [12]. However, reduction in dc link voltage is limited due to large drop in L type interfacing filter. Also, use of L filter makes filter bulky, bigger in size, and has a low slew rate for tracking the reference currents. In literature, LCL filter has been used as front end of VSI instead of L filter [13]–[19]. This scheme provides better reference tracking performance. Also, lower value of passive components ensures that the voltage drop across them are much less. Consequently,

the dc link voltage will also be lesser while using LCL filter.

The advantages of both series capacitor and LCL filter has been proposed in a new DSTATCOM topology. LCL filter is used at the front end of the VSI, which is followed by the series capacitor. Proposed topology has a advantages which reduces, the rating of the dc link voltage, the size of the passive components and provides excellent reference current tracking performance simultaneously. Therefore, the cost, size, weight, and power rating of the DSTATCOM will greatly reduce. A procedure to design LCL filter and series capacitor is presented in detail.

II. TRADITIONAL AND PROPOSED DSTATCOM TOPOLOGY

A. TRADITIONAL TOPOLOGY

Fig.1 describes traditional DSTATCOM topology employed in distribution system. It contains a three-phase, four-wire, two-level, neutral-point-clamped voltage source inverter. It requires two dc storage capacitors. Each leg of the VSI can be controlled independently [8]. v_{sabc} and i_{sabc} are source voltages and source currents of phases *a*, *b*, and *c* respectively. Each phase is composed of resistance R_s and inductance L_s represent feeder impedance. V_{tabc} and i_{labc} are the load terminal voltages and load currents in phases *a*, *b*, and *c* respectively. Loads used here have both linear and non-linear elements. Interfacing inductance and resistance of VSI in each phase are L_f and R_f respectively. DSTATCOM injected currents are i_{fabc} in respective phases. $C_{dc1} = C_{dc2} = C_{dc}$ represents the dc link capacitors, whereas voltages maintained across them are $V_{dc1} = V_{dc2} = V_{dc} = V_{dcref}$ respectively.

Fig.2, integrates DSTATCOM conventional topology with front end L filter replaced by LCL filter, followed by a series capacitor C_{se}. Size of the passive component of the VSI reduces due to the introduction of LCL filter and improves the reference tracking performance. Dc link voltage and the rating of VSI reduces due to the addition of series capacitor to the interfacing filter. Here, R_1 and L_1 represent the resistance and inductance respectively at the filter side, R_2 and L_2 represent the resistance and inductance respectively at the grid side, and *C* is the filter capacitance forming LCL filter part in all three phases. A damping resistance R_d is used in series with *C* to damp out resonance and to provide passive damping to the overall system. i_{f1abc} and i_{f2abc} are currents at filter and grid side in phase *a*, *b*, and *c* respectively. v_{cabc} and i_{cabc} are voltages across and currents through the branch containing series *C* and *Rd* in three phases respectively.

II. EXTRACTION OF REFERENCE CURRENTS USING INSTANTANEOUS SYMMETRICAL COMPONENT THEORY

DSTATCOM is operated such that the source currents are sinusoidal, balanced and in phase with respective voltages. A three-phase, four-wire compensated system is shown in Fig. 1, where the three-phase load may be unbalanced and nonlinear, while the supply voltage may be unbalanced and distorted. A shunt APF (or compensator) and the load are connected at the PCC Average load power and losses are supplied by the source. Direct use of terminal voltages to calculate reference currents will not provide satisfactory compensation, as the source considered here is non-stiff in nature. Using instantaneous symmetrical component theory, three phase reference currents are generated to satisfy load compensation.

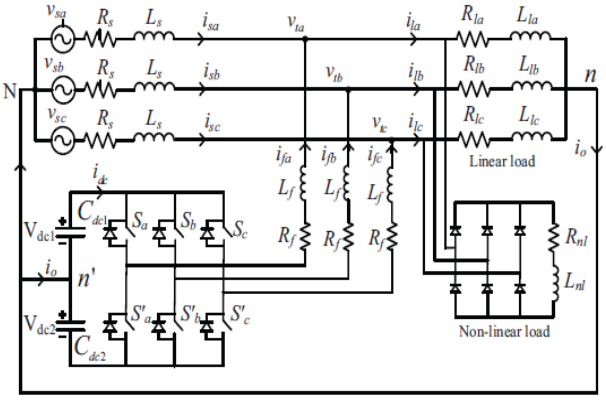


Fig.1 Conventional DSTATCOM Topology.

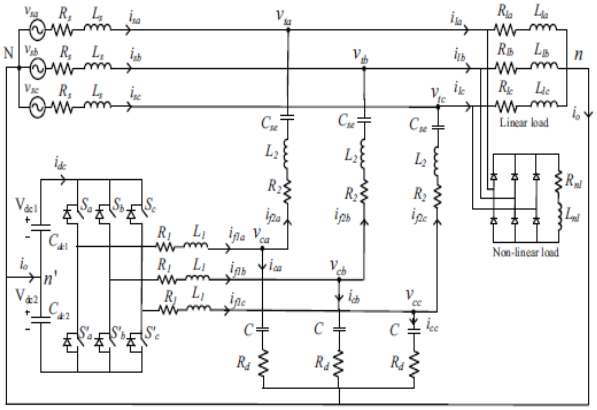


Fig.2 Proposed DSTATCOM topology.

Three phase reference currents are given as follows:

$$i^{*}_{f2a} = i_{la} - i^{*}_{sa} = i_{la} - \frac{v^{+}_{ta1}}{\Delta^{+}_{1}} (R_{lavg} + R_{loss})$$

$$i^{*}_{f2b} = i_{lb} - i^{*}_{sb} = i_{lb} - \frac{v^{+}_{tb1}}{\Delta^{+}_{1}} (R_{lavg} + R_{loss})$$

$$i^{*}_{f2c} = i_{lc} - i^{*}_{sc} = i_{lc} - \frac{v^{+}_{tc1}}{\Delta^{+}_{1}} (R_{lavg} + R_{loss})$$

where, v_{ta1}^{+}, v_{tb1}^{+}, and v_{tc1}^{+} are fundamental positive sequence voltages at the respective phase load terminal and $\Delta_1^{+} = (v_{ta1}^{+})^2+(v_{tb1}^{+})^2+(v_{tc1}^{+})^2$. Here, average load power is represented as P_{lavg} and P_{loss} represents the total losses in the inverter. For better performance during transients, average load power is calculated using a moving average filter. Using PI controller, the total losses in the inverter P_{loss} is computed, which helps in maintaining the dc link voltage $(v_{dc1} + v_{dc2})$at a predefined reference value $(2V_{dcref})$ by drawing a set of balanced current is given as follows:

$$P_{loss} = K_p e + K_i \int e dt$$

Where, K_p, K_i, $e = 2V_{dcref} - (v_{dc1} + v_{dc2})$ are proportional gain, integral gain, and voltage error of the PI controller respectively.
On subtracting actual filter injected currents at grid side from the reference filter currents, an error current control signal, u(t) is obtained. u(t) is regulated around a predefined hysteresis band h using hysteresis current controller (HCC) and IGBT switching pulses are generated as given below:

If u(t) ≥ h, then upper switch of a leg is TURN ON and lower switch is TURN OFF.

else If u(t) ≥ h, then upper switch of a leg is TURN OFF and lower switch is TURN ON.

III. VSI PARAMETER DESIGN

The parameters of VSI are dc bus voltage V_{dc}, dc storage capacitance C_{dc}, and interfacing inductance L_f. Reference tracking performance of a VSI depends upon the parameters of the VSI.

A. Design of Traditional Topology Parameters

1) Reference dc Link Voltage (V_{dcref}) : In order to achieve good tracking performance, the voltage across the dc storage capacitor is assumed to be a source of energy. Here, dc link voltage is maintained at $1.6V_m$, where V_m is maximum of phase voltage. Therefore, the V_{dcref} will be 520V, for a line voltage of 400V.

2) Storage Capacitance (C_{dc}) : Value of dc capacitors are chosen based on its ability to regulate voltage during transients. dc capacitors supply or receive real power to maintain the load power demand during transients. Suppose controller starts working after *n* cycles. The maximum possible energy that capacitor can supply to load or absorb from the load is *n*ST, and it will be equal to change in the stored energy of the capacitor, where system time period is T and S is maximum load rating. hence

$$\frac{1}{2}C_{dc}(V_{dcref}^2 - V_{dc}^2) = nST$$

where, V_{dc} is maximum allowed voltage variation from V_{dcref} during transients. The dc link capacitor value is given as

$$C_{dc} = \frac{2n\,ST}{V_{dcref}^2 - V_{dc}^2}$$

V_{dcref} is 520 V, maximum load rating is taken as 15 kVA, change in dc link voltage during transient is ±20% of V_{dcref}, and *n* is 0.5. Using (3), C_{dc} is found to be 3000 μF.

3) Interfacing Inductance (L_f) : The value of interfacing inductance is chosen such that it provides sufficient rate of change of filter current and reasonably high switching frequency and, such that VSI currents follow the reference currents.
Following equation represents inductor dynamic:

$$L_f \frac{di_{fi}}{dt} = -v_{fc} - R_f i_{fi} + V_{dcref}$$

R_f can be neglected. At maximum switching frequency Inductor is designed to provide good tracking performance which, in HCC, is achieved at the zero of the supply voltage. L_f, Interfacing inductor is given by,

$$L_f = \frac{V_{dcref}}{(2h)(2f_{max})} = \frac{V_{dcref}}{4hf_{max}}$$

where, 2*h* is ripple in the current and maximum switching frequency achieved by HCC is f_{max} .Here, f_{max} is 10 kHz. Ripple in current is taken as 1 A (5% of rated current). Value of interfacing inductance is 26 mH.

B. Design of Proposed Topology Parameters

1) LCL filter design : constraints such as attenuation at switching frequency (f_{sw}), cost of inductor, resonance frequency (f_{res}) and choice of damping resistor (R_d) should be considered while designing values of LCL filter components. Impedance offered by c_{se} will be much lower than that of L_2 at higher frequencies and can be neglected while designing LCL filter parameters.

Consider only L_1 of LCL filter is used. IGBT switching frequency gets lowered when there is a small ripple in current which consequently reduces the switching losses. But the small ripple current results in higher inductance and so more core losses. Therefore to compromise ripple and inductor size, a current ripple of 20% is taken. By using series capacitor, dc link voltage is reduced to as low as 110V. On keeping f_{max} constant at 10 kHz, Value of L_1 comes out to be 2.75mH. In order to restrict switching frequency below 10 kHz, L_1 is chosen to be 3mH.

L_1 is designed to attenuate lower order harmonics and in similar manner L2 and C need to be designed for elimination of higher order harmonics. The information of LCL filter behavior at the higher frequencies is provided by the following transfer functions.

$$\frac{I_{f1}(s)}{V_{inv}(s)} = \frac{s^2 + 1/L_2C}{sL_1(s^2 + (L_1 + L_2/L_1L_2C))}$$

$$\frac{I_{f2}(s)}{V_{inv}(s)} = \frac{1/L_1L_2C}{s(s^2 + (L_1 + L_2/L_1L_2C))}$$

$$\frac{I_{f2}(s)}{I_{f1}(s)} = \frac{1/L_2C}{s^2 + 1/L_2C}$$

Resonance frequency is given by,

$$f_{res} = \frac{1}{2\pi}\sqrt{\frac{1+k}{kL_1C}}$$

Where k = L_2/L_1. Resonance frequency must be greater than the highest order of harmonics current to be compensated. f_{res} taken as 2400 Hz, if 40 is the highest harmonics to be compensated and taking a safety factor of 20%. To ensure low loss and high efficiency, a lower value of k is selected. A higher C will provide a low impedance path for harmonics, but will draw more reactive current from VSI, which increases loss in L_1 and IGBT switch. A smaller capacitance will not provide sufficient attenuation which is compensated by selecting larger inductor. So C = 10 µF is chosen. Finally k = 0.172 and L_2 is found to be 0.6 mH.

Equivalent impedance of the LCL filter approaches to zero at f_{res} and system become unstable. Inserting a resistance R_d in series with a capacitor can prevent this unstablility. To minimize the losses, it is chosen in proportion to capacitive reactance at f_{res}. The reactance offered by C is 6.63 Ω at f_{res}. Since losses in R_d are compensated by taking current from the source, it should be minimized. By taking these into consideration, a resistance is chosen to be 15 Ω, which is twice the reactance offered by C at resonance.

2) Series Capacitor (C_{se}) : The value of C_{se} is chosen in such a way that it should provide a low impedance path for the fundamental frequency current component. Designed of C should be such that it provides a high impedance path for the lower order harmonics. Fundamental current is drawn by the C and it gets neglected at the fundamental frequency.

In simplified circuit, R_1, L_1, R_2, L_2 and C_{se} are connected in series.

$$I_{f1} = \frac{V_{inv1} - V_{t1}}{R_f + j(X_{l1} - X_{se1})}$$

Where, $R_f = R_1 + R_2$, $X_{l1} = \omega_1(L_1 + L_2)$, $X_{se1} = 1/\omega_1 C_{se}$, V_{inv1} is fundamental rms voltage per phase at VSI terminal and V_{t1} is fundamental rms PCC voltage. $V_{inv1}$is given as

$$V_{inv1} = \frac{V_{dc}}{\sqrt{2}}$$

On simplifying,

$$I_{f1} = \frac{(V_{inv1} - V_{t1})R_f - j(V_{inv1} - V_{t1})(X_{l1} - X_{se1})}{R_f^2 + (X_{l1} - X_{se1})^2}$$

Comparing to reactive part, the interfacing resistance are very small and can be neglected. The imaginary part magnitude of the I_{f1} will be

$$I_m[I_{f1}] = -\frac{V_{inv1} - V_{t1}}{X_{l1} - X_{se1}}$$

To inject reactive current from compensator to PCC, rms voltage per phase at the VSI terminal and therefore, dc link voltage must be greater than the terminal voltage. Otherwise, the compensation performance will be dissatisfactory. Maximum injected current only depends upon the dc link voltage due to the absent of series capacitor in the conventional topology. Therefore, dc link voltage is maintained at higher value as compared to terminal voltage. Total impedance provided by the compensator decreases when the series capacitor is inserted in series with filter.

TABLE I: SYSTEM PARAMETERS

System quantities	Values
Source voltage	400 V rms line to line, 50 Hz
Feeder impedance	$Z_s = 1 + j3.14\ \Omega$
Linear load	$Z_{la} = 30 + j62.8\ \Omega$, $Z_{lb} = 40 + j78.5\ \Omega$, $Z_{lc} = 50 + j50.24\ \Omega$
Non-linear load	3-phase full bridge rectifier with a R-L load of $50 + j62.8\ \Omega$
VSI parameters (Traditional topology)	$V_{dc} = 520$ V, $C_{dc} = 3000\ \mu$F, $L_f = 26$ mH, $R_f = 0.1\ \Omega$,
VSI parameters (Proposed topology)	$V_{dc} = 110$ V, $C_{dc} = 3000\ \mu$F, $L_1 = 3$ mH, $L_2 = 0.6$ mH, $R_1 = R_2 = 0.05\ \Omega$, $C_{fc} = 10\ \mu$F
Hysteresis bands (h)	± 0.5 A

Therefore, dc link voltage can be reduced from its reference value for same reactive current injection. Thus, value of series capacitor depends upon the maximum reactive filter current and it extends up to what we want to decrease the dc link voltage. To achieve unity power factor at load terminal, maximum reactive current that a compensator can supply must be same as that of maximum load reactive current. When it offer minimum impedance ($Z_{lmin} = R_{lmin} + jX_{lmin}$) i.e., at full load, load current will be maximum. Therefore, maximum fundamental current drawn by the load is given as,

$$I_{lmax} = \frac{V_{t1}}{R_{lmin} + jX_{lmin}}$$

Calculating imaginary load current magnitude

$$\frac{V_{t1}X_{lmin}}{Z_{lmin}^2} = \frac{V_{inv1} - V_{t1}}{X_{l1} - X_{se1}}$$

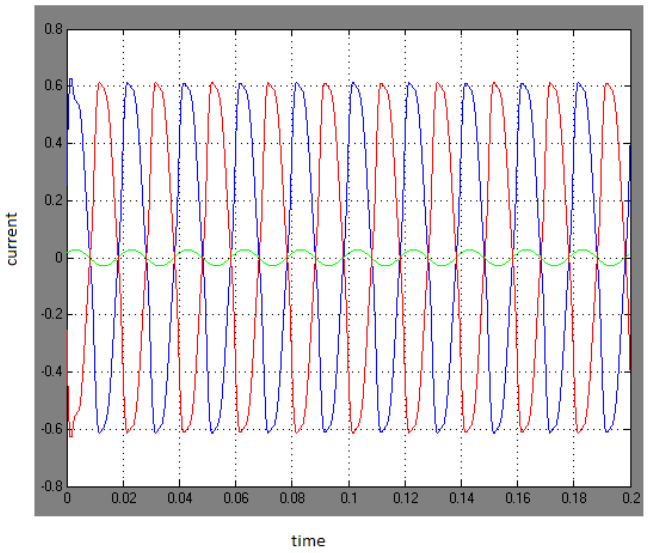
The value of X_{se1} is given by,

$$X_{se1} = X_{l1} - \frac{V_{inv1} - V_{t1}}{I_{lmax}\sqrt{1 - pf_{lmin}^2}}$$

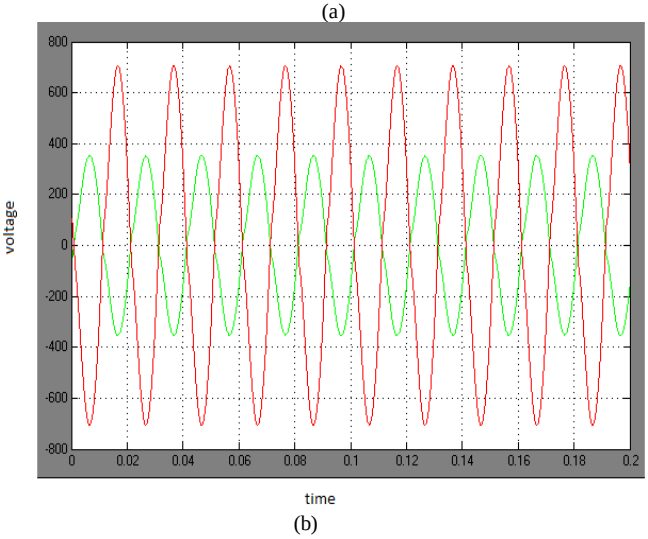
Based on values in Table I, where the phase b requires maximum reactive current having minimum impedance, value of series capacitor can be computed. C_{se} is found to be 46.13 μF. C_{se} is taken as 50 µF for practical considerations.

IV. RESULTS AND DISCUSSIONS

Lower rating of the VSI, smaller value of interfacing filter, lower overall size, cost and weight are the advantages of proposed topology over traditional topology. All these advantages are verified in MATLAB/ Simulink.

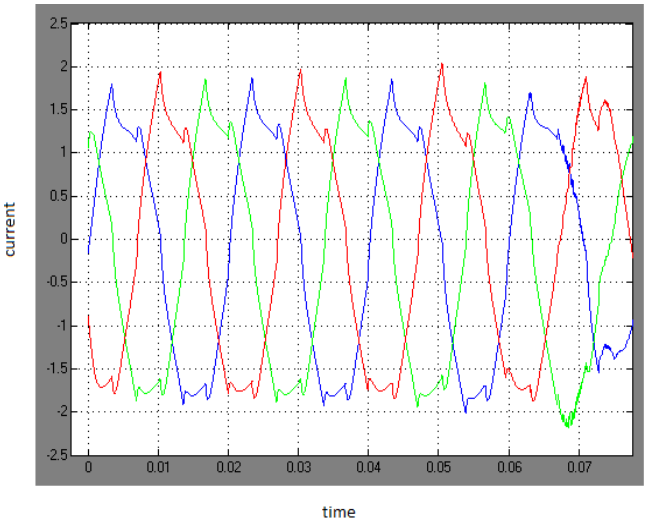


(a)

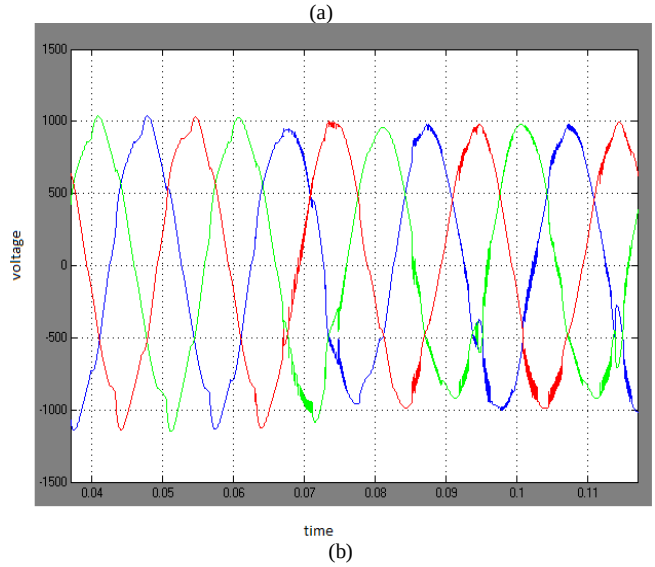


(b)

Fig 3: Before compensation (a) Source currents (b) PCC voltages.

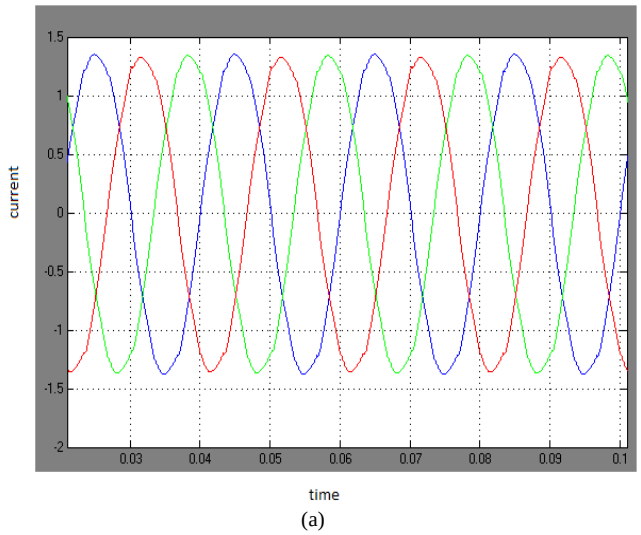


(a)

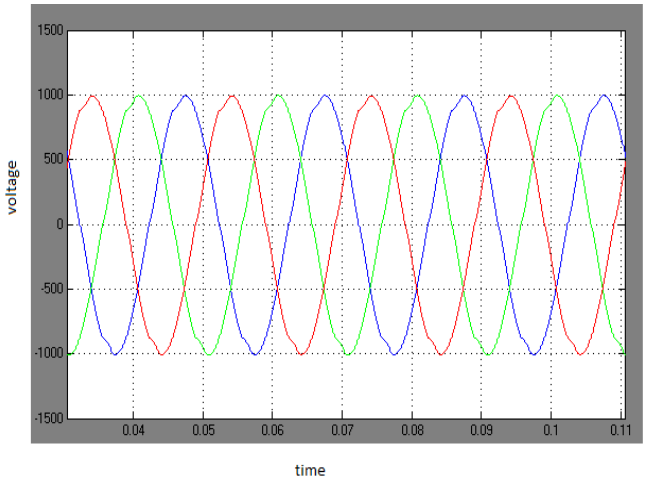


(b)

Fig. 4. In traditional topology (a) Source currents (b) PCC voltage.



(a)



(b)

Fig 5: Proposed Topology (a) Source Currents (b) PCC Voltage

Fig.3 presents the source currents and PCC voltages before compensation. The source currents and voltages are unbalanced and sinusoidal. The performance of traditional topology with L filter is presented in Fig. 4. shows the source currents and PCC voltages in traditional topology. The three phase voltages and currents are balanced and sinusoidal. Fig.5 (a) shows the three phase compensated source currents which are balanced, sinusoidal and have negligible switching ripple as compared to traditional topology. Neutral current is nearly zero. Fig.5 (b) shows the three phase compensated PCC voltages with greatly reduced switching harmonics. Also, unity power factor is achieved, in showing that the respective phase voltages are in phase with respective source currents. Table II , it is clear that the three phase source currents as well as in PCC voltage is sufficient for the DSTATCOM to achieve its current compensation performance.

Table II: Percentage THDs in Source currents and Terminal voltages

System configuration	I_{SA}	I_{SB}	I_{SC}	V_{TA}	V_{TB}	V_{TC}
Without compensation	16.41	16.44	19.04	8.55	11.45	8.73
Traditional Topology	10.71	9.21	10.71	6.49	6.51	6.49
Proposed Topology	3.29	3.91	3.66	2.58	3.89	2.67

The performance of traditional DSTATCOM topology with L filter is presented. It can be observed that both the source currents and terminal voltages contain switching frequency of the VSI. Voltage across the each capacitor is maintained at 520V whereas, total dc link voltage is maintained at 1040 V using PI controller. Based on designed procedure, L_1 = 3 mH, L_2= 0.6 mH, C = 10 µF, R_d = 15 Ω, C_{se} = 50 µF, and Vdc = 110 V are obtained. Series capacitor is designed based on phase-b load current because it has maximum current among all three phases. Load and source parameters are given in Table I. Source currents are in phase with their respective phase voltages and unity power factor is achieved.

Table III: Comparison of VSI Parameters

Parameters	Traditional topology	Proposed Topology	Percentage Reduction
Inductor value	26 mH	3.6 mH	86.15
Voltage at DC bus	1040 V	220 V	78.85

From Table II, clear that the percentage THDs in three phase source currents as well as in PCC voltages are considerably lesser in proposed topology. Also, these waveforms confirm that the reduced dc link voltage is sufficient for the DSTATCOM to achieve its current compensation performance. Here, dc link voltage is 110 V which is only 21.15% of traditional topology. Therefore, total power rating of VSI is reduced by 78.85% while achieving enhanced current compensation capability. In addition to this, the overall filter size is also significantly reduced. Comparative analysis of VSI parameters is presented in Table III.

VI. CONCLUSION

A new DSTATCOM topology, comprising of a LCL filter at the front end of voltage source inverter followed by a series capacitor has been proposed. A procedure to design DSTATCOM parameters is presented. By using a much lower value of dc link voltage as well as interfacing filter inductor, it results such that the proposed topology provides superior current compensation compared to traditional topology. Therefore, the cost, weight, and power rating of the DSTATCOM will be significantly reduced to traditional topology.

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